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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,556	12/19/2001	Kenneth Blemel	97Y-84435	2328

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EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 12/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,556	BLEMEL, KENNETH	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *7-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,11 and 12* is/are rejected.

7)☒ Claim(s) *3,5,6 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-6 and 11-13, drawn to multi-chip module instrument controller, classified in class 713, subclass 500.

II. Claims 7-10, drawn to multi-chip module instrument controller, classified in class 713, subclass 323.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as multi-chip module instrument controller with power management providing automatic activation/deactivation of processor based on an external signal. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with James Brueggemann on 11/24/2004 a provisional election was made with traverse to prosecute the invention of I, claims 1-6 and 11-13. Affirmation of this election must be made by applicant in replying to this Office action. Claims 7-10 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation "microprocessor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lyke in view of Clotier and DaCosta.

Re claim 1, Lyke discloses a multi-chip module instrument controller (column 1, lines 58-62, Fig. 1) comprising a non-volatile memory storage component for program and data storage (column 3, line 66, column 4, lines 14 and 15, Fig.1); a large volatile memory storage component for additional program and data storage (column 4, lines 35-37, Fig. 1); a processor coupled to both said non-volatile memory storage (Fig. 1) said processor capable of high-frequency and low-frequency operations (column 4, lines 42-44); at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations (column 4, lines 42-44, Fig. 1); a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing said analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing said digital inputs to processor (column 3, lines 28-33, Fig. 1).

Lyke fails to disclose an embedded memory for storing an initialization program and a field programmable gate array coupled to the processor for parallel processing.

DaCosta teaches embedded CPU registers (paragraph 0028, lines 1-5, paragraph 0029, lines 12-14, FIG. 2) for storing operating system software (paragraph 0034, lines 2-5) that enables the processor to start processing without first copying the application software into RAM. In DaCosta, the use of embedded non-volatile CPU registers provides for fast bootup and shutdown with information preservation when the system is powered down (paragraph 0015, lines 1-15, paragraph 30, lines 4-7). It would have been obvious to one of the ordinary skill in the art at the time of applicant's invention to incorporate the embedded registers and bootup sequence, as suggested by

DaCosta for the multi-chip module instrument controller disclosed by Lyke in order to store an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory.

Cloutier teaches a multiprocessor based on a multidimensional array of field programmable gate arrays (FPGAs) (column 2, lines 9-13, FIG. 1) adapted to function as a parallel processor (column 2, lines 65-67). In Cloutier, the multiprocessor provides improved data processing for applications requiring large number of operations (column 1, line 32-35). It would have been obvious to one of the ordinary skill in the art at the time of applicant's invention to use the FPGA-based processing elements, as suggested by Cloutier for the multi-chip module instrument controller disclosed by Lyke in order to run independent processes in parallel with the processor.

Re claim 2, Lyke discloses the multi-chip instrument controller, further comprising a plurality of analog outputs, each being controlled by an independent digital-to-analog converter, each of said independent digital-to-analog converters being configured to convert from one of at least two possible depths to analog (column 3, lines 63-65).

Re claim 11, Lyke discloses a method using multi-chip module instrument controller (Fig.1) receiving a plurality of analog inputs, digitizing said analog inputs at one of at least two possible bit depths (thereby generating digital inputs) (column 3, lines 28-33), providing the first portion of said digital inputs to said processor (Fig. 1), performing digital signal processing on said first portion of said digital inputs utilizing the processor (Fig. 1).

Lyke fails to disclose multiple parallel signal processing utilizing both processor and a field programmable gate array.

Cloutier teaches a multiprocessor based on a multidimensional array of field programmable gate arrays (FPGAs) (column 2, lines 9-13, FIG. 1) adapted to function as a parallel processor (column 2, lines 65-67). In Cloutier, the multiprocessor provides improved data processing for applications requiring large number of operations (column 1, line 32-35). It would have been obvious to one of the ordinary skill in the art at the time of applicant's invention to use the FPGA-based architecture, as suggested by Cloutier for the method disclosed by Lyke in order to achieve multiple signal processing.

Re claim12, Lyke discloses the method as per claim 11, further comprising the additional steps of providing at least two internal oscillator signals to the processor for low-speed and high-speed digital signal processing operations (column 4, lines 42-44, Fig. 1).

Claim Objections

Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 4 includes every limitations of the parent claim 1.

Allowable Subject Matter

Claims 3, 5, 6, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claim 3, the prior art fails to disclose or suggest "first portion of the gates configured to perform signal processing; and second portion of the gates configured to operate as a signal distribution matrix".

Re claim 5, the prior art fails to disclose or suggest "resettable digital real-time quartz controlled clock for accurate date and time stamping of date and time stamping of data before it is stored in the non-volatile memory".

Re claims 6 and 13, the prior art fails to disclose or suggest "a portion of the gates in the field programmable gate array are configured to operate as an internal embedded power converter".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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